Patent Claims

1. A microelectronic structure having
- a base substrate (5); and
- at least one barrier layer (25, 30) above the base substrate (5);
characterized in that
an adhesion layer (20) is arranged between the base substrate (5) and the barrier layer (25, 30), the adhesion layer (20) containing at least one material from the group comprising titanium, zirconium, hafnium, cerium, tantalum, vanadium, chromium, niobium, tantalum nitride, titanium nitride, tantalum silicide nitride and tungsten silicide.

2. The microelectronic structure as claimed in claim 1, characterized in that the base substrate (5) is at least partly composed of an insulating material (50, 55) and has at least one opening (10), which completely penetrates through the insulating material (50, 55) of the base substrate (5) and is filled with at least one conductive material (8, 9), and in that the adhesion layer (20) is seated directly on the conductive material (8, 9).

3. The microelectronic structure as claimed in claim 2, characterized in that the adhesion layer (20) is additionally seated directly on the insulating material (50, 55) of the base substrate.

4. The microelectronic structure as claimed in claim 2 or 3, characterized in that the insulating material (50, 55) of the base substrate (5) is composed of silicon nitride or silicon oxide.

5. The microelectronic structure as claimed in one of the preceding claims, characterized in that the barrier layer (25, 30) has an oxygen-containing iridium layer (25), which can be fabricated by means of a sputtering process in an oxygen-containing atmosphere at a temperature of at least 250°C, the proportion by volume of oxygen in the atmosphere being between 2.5% and 15%.

6. The microelectronic structure as claimed in one of the preceding claims, characterized in that the barrier layer (25, 30) has an oxygen barrier layer (30).

7. The microelectronic structure as claimed in claim 6, characterized in that the oxygen barrier layer (30) is composed of a conductive metal oxide.

8. The microelectronic structure as claimed in claim 7, characterized in that the conductive metal oxide is composed of iridium dioxide or ruthenium dioxide.

9. The microelectronic structure as claimed in one of the preceding claims, characterized in that a metal-containing electrode layer (35) covers the oxygen barrier layer (30).

10. The microelectronic structure as claimed in one of claims 1 to 9, characterized in that the adhesion layer (20) is seated directly on the opening (10) in the base substrate (5) and partly on the insulating material (50, 55) of the base substrate (5).

11. The microelectronic structure as claimed in claim 10, characterized in that the conductive material (8, 9) in the opening (10) of the base substrate (5) is composed of at least

one metal silicide at least in the contact region with respect to the adhesion layer (20).

12. The microelectronic structure as claimed in one of claims 1 to 9, characterized in that a metal silicide layer (9) is arranged on the base substrate (5) directly between the adhesion layer (20) and the opening (10).

13. The microelectronic structure as claimed in either of claims 11 and 12, characterized in that the metal silicide layer (9) contains at least one silicide from the group yttrium silicide, titanium silicide, zirconium silicide, hafnium silicide, vanadium silicide, niobium silicide, tantalum silicide, chromium silicide, molybdenum silicide, tungsten silicide, iron silicide, cobalt silicide, nickel silicide, palladium silicide, platinum silicide and copper silicide.

14. The microelectronic structure as claimed in one of claims 9 to 13, characterized in that the metal-containing electrode layer (35) is covered by a dielectric, ferroelectric or paraelectric metal-oxide-containing layer (40).

15. A microelectronic structure having
- a base substrate (5), which is at least partly composed of an insulating material (50, 55) and in which is arranged an opening (10), which is filled with at least one conductive material (8, 9) and completely penetrates through the insulating material (50, 55) of the base substrate (5), the conductive material (8, 9) terminating flush with the insulating material (50, 55);
- a barrier layer (25, 30) on the base substrate (5), said barrier layer comprising an iridium dioxide layer (30) and an oxygen-containing iridium layer (25), the oxygen-containing

iridium layer (25) being able to be fabricated by means of a sputtering process in an oxygen-containing atmosphere at a temperature of at least 250°C, and the proportion by volume of oxygen in the oxygen-containing atmosphere being between 2.5% and 15%;
- an adhesion layer (20) above the opening (10) directly between the base substrate (5) and the barrier layer (25, 30), the adhesion layer (20) containing at least one material from the group comprising titanium, zirconium, hafnium, cerium, tantalum, vanadium, chromium, niobium, tantalum nitride, titanium nitride, tantalum silicide nitride and tungsten nitride; and
- a noble metal layer (35) on the barrier layer (25, 30).

16. A microelectronic structure having
- a base substrate (5), which is at least partly composed of an insulating material (50, 55) and in which is arranged an opening (10), which is filled with at least one conductive material (8) and completely penetrates through the insulating material (50, 55) of the base substrate (5), the conductive material (8) terminating flush with the insulating material (50, 55);
- a metal silicide layer (9) above the opening (10) directly on the base substrate (5);
- a barrier layer (25, 30), which is arranged above the metal silicide layer (9) and comprises an iridium dioxide layer (30) and an oxygen-containing iridium layer (25), the oxygen-containing iridium layer (25) being able to be fabricated by means of a sputtering process in an oxygen-containing atmosphere at a temperature of at least 250°C, and the proportion by volume of oxygen in the oxygen-containing atmosphere being between 2.5% and 15%;
- an adhesion layer (20) directly between the metal silicide layer (9) and the barrier layer (25, 30), the adhesion layer

(20) containing at least one material from the group comprising titanium, zirconium, hafnium, cerium, tantalum, vanadium, chromium, niobium, tantalum nitride, titanium nitride, tantalum silicide nitride and tungsten silicide; and
- a noble metal layer (35) on the barrier layer (25, 30).

17. A process for fabricating a microelectronic structure having
- a base substrate (5);
- at least one barrier layer (25, 30) above the base substrate (5); and
- an adhesion layer (20) between the base substrate (5) and the barrier layer (25, 30), the adhesion layer (20) containing at least one material from the group comprising titanium, zirconium, hafnium, cerium, tantalum, vanadium, chromium, niobium, tantalum nitride, titanium nitride, tantalum silicide nitride and tungsten silicide,
characterized by the steps of:
- providing the base substrate (5);
- applying the adhesion layer (20) to the base substrate (5); and
- applying the barrier layer (25, 30) to the adhesion layer (20).

18. The process as claimed in claim 17, characterized in that the adhesion layer (20) is applied by means of a sputtering process.

19. The process as claimed in claim 17, characterized in that the adhesion layer (20) is applied by means of a CVD process.

20. The process as claimed in one of claims 17 to 19, characterized in that the barrier layer (25, 30) has an oxygen-containing iridium layer (25), which is applied by

means of a sputtering process in an oxygen-containing atmosphere at a temperature of at least 250°C, the proportion by volume of oxygen in the atmosphere being between 2.5% and 15%.

21. The process as claimed in claim 20, characterized in that the barrier layer (25, 30) has, in addition to the oxygen-containing iridium layer (25), an iridium dioxide layer (30), which is applied to the oxygen-containing iridium layer (25).

22. The process as claimed in one of claims 17 to 21, characterized in that a metal-containing electrode layer (35) is applied to the barrier layer (25, 30) and a dielectric, ferroelectric or paraelectric metal-oxide-containing layer (40) is applied to said electrode layer.